Universidade de Brasília – UnB
Faculdade UnB Gama – FGA
Engenharia Eletrônica

Basic building blocks for Power Management Integrated Circuits

Autor: Diego Galdino Mendonça
Orientador: Doutor Sandro Augusto Pavlik Haddad

Brasília, DF
2022

Diego Galdino Mendonça

Basic building blocks for Power Management Integrated Circuits

Monografia submetida ao curso de graduação em Engenharia Eletrônica da Universidade de Brasília, como requisito parcial para obtenção do Título de Bacharel em Engenharia Eletrônica.

Universidade de Brasília – UnB

Faculdade UnB Gama – FGA

Orientador: Doutor Sandro Augusto Pavlik Haddad

Brasília, DF

2022

Diego Galdino Mendonça
Basic building blocks for Power Management Integrated Circuits/ Diego Galdino Mendonça. – Brasília, DF, 2022-
50 p. : il. (algumas color.) ; 30 cm.

Orientador: Doutor Sandro Augusto Pavlik Haddad

Trabalho de Conclusão de Curso – Universidade de Brasília – UnB
Faculdade UnB Gama – FGA , 2022.

1. CMOS. 2. PMIC. I. Doutor Sandro Augusto Pavlik Haddad. II. Universidade de Brasília. III. Faculdade UnB Gama. IV. Basic building blocks for Power Management Integrated Circuits

CDU 02:141:005.6

Diego Galdino Mendonça

Basic building blocks for Power Management Integrated Circuits

Monografia submetida ao curso de graduação em Engenharia Eletrônica da Universidade de Brasília, como requisito parcial para obtenção do Título de Bacharel em Engenharia Eletrônica.

Trabalho aprovado. Brasília, DF, 31 de março de 2023:

Doutor Sandro Augusto Pavlik Haddad
Orientador

Doutor Gilmar Silva Beserra
Convidado 1

Doutor Wellington Avelino do Amaral
Convidado 2

Brasília, DF
2022

I dedicate this work to all the people who always believed in me, especially my parents and sister, who tried to give me the opportunities they never had, hoping I could accomplish the dreams they never could. I also appreciate the support from Professor Sandro Haddad, Professor Gerardo Pizo, my friend Haniel Lima and the boys from SAMU along with all the university's professors and all the friends I made there, because without them I could never take it this far.

Resumo

Nesse trabalho, utilizamos como referencial o modelo do MOSFET compacto avançado (ACM) que se baseia fortemente no funcionamento físico do transistor, visando detalhar o projeto de blocos básicos utilizados na construção de unidades de gerenciamento de energia (PMU) e circuitos integrados de gerenciamento de energia (PMIC). Os blocos abordados foram o retificador Dickson, retificador de pares cruzados, fonte de corrente autopolarizada e amplificador operacional *folded cascode*.A metodologia adotada emprega desde a explicação do funcionamento teórico dos blocos individuais assim como os cálculos teóricos, quando aplicáveis, até os resultados simulacionais para avaliação do cumprimento dos requisitos estabelecidos. Com os circuitos projetados podemos vislumbrar um ponto de vista abrangente em relação ao passos de projeto envolvidos no desenvolvimento de circuitos analógicos/mistos compreendidos em processos de fabricação de chips integrados.

Palavras-chave: CMOS; PMIC; PMU; Projeto;

Abstract

In this work, we use as reference the advanced compact MOSFET (ACM) model that relies heavily on the physical operation of the transistor, aiming to detail the design of basic blocks used in the construction of power management units (PMU) and power management integrated circuits (PMIC). The blocks addressed were the Dickson rectifier, cross-coupled rectifier, self biased current source and folded cascode operational amplifier. The methodology adopted employs everything from explanation of the theoretical operation of the individual blocks as well as theoretical calculations, where applicable, to simulation results for evaluation of compliance with the established requirements. With the designed circuits we can glimpse a comprehensive viewpoint regarding the design steps involved in the development of analog/mixed circuits entangled in integrated chip fabrication processes.

Key-words: CMOS; Design; PMIC; PMU;

Lista de ilustrações

Lista de tabelas

Lista de abreviaturas e siglas

ACM	Advanced Compact Mosfet
AC	Alternated current
DC	Direct current
DRC	Design rule check
GBW	Gain–bandwidth product
LDO	Low-dropout regulator
LVS	Layout versus schematic
MOSFET	Metal oxide semiconductor field effect transistor
PMIC	Power management integrated circuit
PMU	Power management unit
SBS	Self biased structure
SBCS	Self biased current source
SCM	Self cascode mosfet
VDD	Voltage Drain-to-Drain

Sumário

1 Introduction

The development of small chips in the last decades enabled our lifestyle and society as a whole to be changed through the use of big data generated by Internet usage. It is done mainly through data sensing, gathering, processing, storing, and networking through wired and wireless connections to the World Wide Web (WWW). The sudden growth of this field of minimalist electronic devices created the demand for more efficient, environmentally benign, and sustainable energy management units. (HELLA; MERCIER, 2016)

Power management refers to the management of power-related activities in any electronic device, which include generation, storage, distribution, and control of regulated voltages and currents required to correctly operate the host system. (DAS, 2017). Portable devices frequently comprise several sub-circuits that should be supplied with different voltage levels which are not the same as the battery's voltage level so the power management integrated chip (PMIC) or power management unit (PMU) is the section of the system responsible for these adjustments. (SAFARI, 2012).

A power management unit can be composed of several different blocks that may serve many distinct purposes, the most common PMU blocks are listed below.

- POR - Power-On Reset, this is a block that provides a reset signal to the chip when the supply voltage ramps up so that the circuit always starts in a known state by resetting all inner registers and circuits (YASUDA; YAMAMOTO; NISHI, 2001). The most common topology is typically a delay element combined with a Schmitt trigger.

- LDO - Low-Dropout Regulator, The main purpose of an LDO is to provide an approximately constant supply voltage to other circuits and to isolate circuits from each other to avoid cross-talk happening via the supply lines (KRUISKAMP; BEUMER, 2008). It is often implemented using a pass transistor, and a combination of an operational amplifier, a voltage reference(BANDGAP), and a voltage divider to compose negative feedback to adjust the output voltage.

- DC-DC Converter. A DC-DC converter is used to transfer DC voltage from the input voltage to a different output voltage level (DANCY; AMIRTHARAJAH; CHANDRAKASAN, 2000). It is often implemented using a switching regulator such as a Buck or boost converter. Those blocks therefore can be made by a combination of several different blocks such as voltage references(BANDGAP), voltage rectifiers, current references, hysteretic comparators, sawtooth wave generators, current sensing circuits, feedback compensation circuits (types ranging from I to III), etc...

In this thesis, we will be focusing on the development of a few of the basic blocks that could be used to compose part of a Buck DC-DC converter. More specifically we will be developing a current source, a voltage rectifier, and an operational amplifier.

1.1 Objectives

This thesis focuses on the development of a rectifier, a folded cascode, and a current sink block for power management purposes.

1.1.1 Specific objectives

The following goals are the expected results from this research:

- Design and validate a Dickson charge pump rectifier for certain specifications of input, output voltages, and loads and validate the results through simulations on CADENCE Spectre.
- Design and validate a Cross-coupled rectifier for the same circumstances as the Dickson charge pump for comparison between the topologies.
- Design and validate a Folded cascode amplifier to be used on the topology of other basic PMU blocks in near future work.
- Design and validate a Self Biased Current Source to be used on the topology of other basic PMU blocks in near future work.

1.1.2 Circuit specifications

The circuits presented in this work had different specific purposes for their development, even though they all share the common objective of this thesis, being to design simple common blocks that are widely used in the construction of power management units as a showcase of the CMOS design procedure using the ACM model.

The rectifier blocks were designed as part of the design of a power management unit for an ultra-low power integrated circuit with UWB communication, therefore the input and output specifications were all fed from the project's needs.

Another block that was initially designed for the same reason as the rectifier is the folded cascode amplifier. It was an amplifier that was meant to be used on the feedback loop of a bandgap for the same project cited above. For that reason, there were some set specifications to be reached as the open loop gain, GBW, and PSRR. But differently from the rectifier block the folded cascode ended up not being used in the project and therefore the steps involved in layout design weren't needed.

On the other side, the current source designed wasn't meant to be used in the project, the chosen specification of $1\mu A$ was selected for being considered a fairly common current source output current.

1.2 Personal Motivation

The reason behind this theme choice is pretty simple after learning about the Advanced Compact MOSFET Model for circuit design I was eager to learn more and dive into efficient power management circuits, associated with observations on the international vacancies for analog circuit design engineers this seemed like a pretty reasonable place to start the research on analog and mixed-signal circuits.

1.3 Methodology

1.3.1 General design approach

Two main approaches are commonly used in the development of analog/mixed-signal circuits, they are the Top-Down and Bottom-Up methodologies. Those will be briefly explained in the following paragraphs.

Top-Down methodology refers to a design routine that starts with the definition of the high-level requirements of a system and then proceeds to refine the design by breaking it down into smaller subsystems. In the context of CMOS design, the top-down methodology involves defining parameters such as input-output characteristics, power consumption, and size constraints. The designer then progressively refines the design by selecting appropriate building blocks and then optimizing their parameters using simulations and design rules.

On the other hand, the Bottom-Up is a design approach that starts with the smallest building blocks of a system, such as transistors and capacitors, and gradually combines them to form higher-level subsystems until finally form the complete system. In the context of CMOS design, the bottom-up methodology involves starting with the design of individual transistors and their interconnections and then combining them to form the most basic blocks, such as current mirrors, logic gates, single-stage amplifiers, etc. These basic blocks then are combined to form more complex building blocks, such as the ones described in this thesis. The designer typically uses simulation tools to verify the correctness and performance of each subsystem before integrating them into the final circuit.

This thesis uses a combination of both, also known as a meet-in-the-middle development method as there are Bottom-up and Top-down aspects to the way the circuits

are designed and presented.

All circuits were developed using the UMC 0.18 μm process and simulated within the Cadence virtuoso environment through the licenses provided to the University.

1.3.2 Specific design methodology

For the blocks presented in this thesis, there were basic steps taken to properly design them in an organized manner.

1. Theoretical reference research.
2. Topology choice.
3. Theoretical calculations and design.
4. Simulations to verify the theoretical design.
5. Design refining optimizations to make up theoretical and simulational discrepancies.

First, there was a theoretical reference evaluation to acknowledge the possible topologies to be used and a proper explanation of their basic functioning principles.

With that out of the way in some cases as the rectifiers, where the Top-Down methodology was utilized, the overall parameters needed were taken into account as there were clear characteristics that the final rectifier was supposed to fulfill for example the input signal of a 900MHz wave coming from the antenna and the output signal that should be around 1.5 Volts or so. And then the circuit was simulated with those objectives in mind.

For other circuits as the current sink, the development method was more Bottom-up orientated but still had an important top-down parameter set beforehand namely the output current of 1 μA. Apart from this parameter the way the chosen topology works is based on an equilibrium point reached with the combination of 2 SCM blocks with different inversion levels, so they were designed first and then combined later on with the current mirrors and the self-biased structure (SBS) in the middle.

1.3.3 Simulation

For each of the different blocks, there was a specific simulation setup to test it in an appropriate manner simulating the operating conditions that it was supposed to meet. For example, to test the Dickson rectifier the input signal was a 900MHz sine wave with 500 mV of amplitude and the output signal was connected to a PMOS transistor as its output in the project was most certainly the low-dropout PMOS transistor of an LDO block.

1.3.4 Extra steps for the Cross-coupled Rectifier

The Cross-coupled rectifier block needed some special attention as it was designed to be part of a bigger project that was sent to be made on a chip. For that reason, a few extra steps were needed to make sure it was going to work successfully. One of the important steps needed to make sure a design can work properly is the evaluation of the PVT corners simulation. Those were made for the specified parameters of 0º C, 27º C, and 100º C, also changing the process ranging from SS, TT, and FF, and other block-specific parameters as the input signal amplitude in the case of the cross-coupled rectifier. Those simulations assure that the design variables and operation conditions are accounted for and can be evaluated appropriately when the chip is finally delivered.

Another important step was the layout of the chip, even though this kind diverges a little from the main goal of this thesis the layout of the cross-coupled rectifier was made so it could be further tested through DRC(Design Rule Check), LVS(Layout versus schematic) and post layout simulations. All of Those steps were not included originally in this thesis but the final layout can be seen in the appropriate result section.

1.4 File structure

This document is divided into 4 chapters with the first being this introduction. The second chapter gives a brief explanation of the operational principles of the chosen topologies. The third chapter walks through the design process and results accomplished, and the fourth one concludes the analysis and gives a glimpse of the plans for future works.

2 Theoretical References

2.1 ACM

The original paper from 1998 (CUNHA; SCHNEIDER; GALUP-MONTORO, 1998) introduced a charge-based MOSFET (Metal Oxide Semiconductor Field Effect Transistor) model that was further improved in 2007 (GALUP-MONTORO et al., 2007) and most recently received small tweaks to truly live up to it's name as a real compact MOSFET model based in 4 simple parameters. (ADORNES et al., 2022)

ACM or Advanced Compact MOSFET is a model for analysis and design of circuits based on the device physics that can describe the behavior of the MOSFET in all regions of operation. (GALUP-MONTORO et al., 2007).

The Advanced Compact MOSFET model introduces the concept of inversion levels to describe the drain current I_D as in (2.1).

$$I_D = I_F - I_R \tag{2.1}$$

I_F is the direct component of the drain current based on the voltages of the gate and source in prospect to the bulk terminal, respectively V_{GB} and V_{SB}, and I_R is the reverse component of the drain voltage based on the voltages of the gate and drain in prospect to the bulk terminal, respectively V_{GB} and V_{DB} as in (2.2) and (2.3). (ADORNES et al., 2022)

$$I_F = F(V_{GB}, V_{SB}) \tag{2.2}$$

$$I_R = F(V_{GB}, V_{DB}) \tag{2.3}$$

The specific current (I_S) is based on the device geometry and the technological parameters expressed in (2.4).

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{2.4}$$

Where μ is the carrier mobility (μ_n for the NMOS transistor and μ_p for the PMOS transistor), C'_{ox} is the oxide capacitance per unit area, n is the slope factor, ϕ_t is the thermal voltage, W is the width and L is the length of the transistor channel.

Together the technological parameters determine the so-called sheet normalization current I_{SH} in (2.5) that can be experimentally extracted from simulations.

$$I_{SH} = \frac{\mu C'_{ox} n \phi_t^2}{2} \tag{2.5}$$

So we have the specific current I_S defined as in (2.6).

$$I_S = I_{SH} \frac{W}{L} \tag{2.6}$$

Therefore using the specific current I_S we can define the drain current based on the direct and reverse inversion levels i_f and i_r as in 2.7.

$$I_D = I_S(i_f - i_r) \tag{2.7}$$

We use i_f to represent the direct inversion level easily so that for $i_f \leq 1$ the device is in weak inversion, for $i_f \geq 100$ the device is in strong inversion and for values in between the device is in the moderate inversion.

The unified current-control model (UICM) expressed in (2.8) states the relationship between the inversion levels $i_{f(r)}$ and the voltages at the device terminals.

$$\frac{V_P - V_{S(D)B}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + ln(\sqrt{1 + i_{f(r)}} - 1) \tag{2.8}$$

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n} \tag{2.9}$$

Where V_P is the pinch-off voltage, V_{T0} is the equilibrium threshold voltage and σ is the DIBL factor.

To guarantee that the transistors are in the saturation region, there is also the approximation for the minimum value for $V_{D,sat}$ as in (2.10).

$$V_{D,sat} = \phi_t\Big(\sqrt{1 + i_f} + 3\Big) \tag{2.10}$$

To summarize the design-oriented 4 parameter expressions for the long-channel MOSFET in saturation we have the equations for the transconductances gms, gmd, gm and intrinsic frequency f_T in (2.11), (2.12), (2.13) and (2.14).

$$\phi_t \frac{g_{ms}}{I_{D,sat}} = \Big(1 - \frac{\sigma}{n}\Big) \frac{2}{\sqrt{1 + i_f} + 1} \tag{2.11}$$

$$\phi_t \frac{g_{md}}{I_{D,sat}} = \frac{\sigma}{n} \frac{2}{\sqrt{1 + i_f} + 1} \tag{2.12}$$

$$\phi_t \frac{g_m}{I_{D,sat}} = \frac{1}{n} \frac{2}{\sqrt{1 + i_f} + 1} \tag{2.13}$$

$$f_T = \frac{\mu\phi_t}{\pi L^2}\left(\sqrt{1+i_f}-1\right) \tag{2.14}$$

With the model established the parameters needed to use the ACM equations are the DIBL factor σ, the sheet current I_{SH}, the slope factor n, and the equilibrium threshold voltage V_{T0}. All of those can be experimentally extracted from a desired technology with the usage of proper topologies and simulations. (ADORNES et al., 2022)

2.1.1 Current Mirrors

To further understand the usage of the ACM model in a common circuit, let's take the example of the low voltage cascode current mirror as shown in Fig. (1) as we use the design equations to establish the appropriate bias circuit.

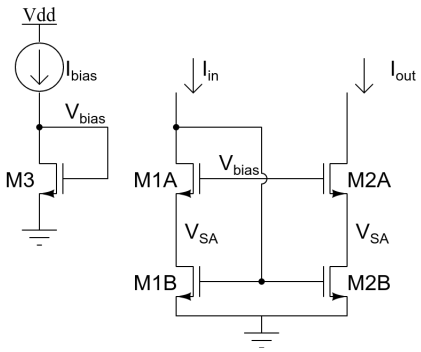

Figura 1 – Low voltage cascode current mirror

Source: Author

Assuming a pre established 1:1 mirror the parameters as current, aspect ratio and inversion levels are already defined and making $M1A = M1B = M2A = M2B$ we have $i_{f1a} = i_{f1b} = i_{f2a} = i_{f2b} = i_{f1}$. The minimum voltage to guarantee saturation of M1B and M2B is given from (2.10) so it's wise to add a small ΔV margin to set V_{SA} apart from the limit. For this example let's choose an additional margin of $\Delta V = 4\phi_t$ making V_{SA} as in equation (2.16).

$$V_{SA} = \phi_t\left[\sqrt{1+i_{f1}}+3\right] + \Delta V \tag{2.15}$$

$$V_{SA} = \phi_t\left[\sqrt{1+i_{f1}}+7\right] \tag{2.16}$$

Applying UICM (2.8) to the topside mirror, we have the equation (2.17).

$$V_{PA} - V_{SA} = \phi_t\left[\sqrt{1+i_{f1}} - 2 + ln\left(\sqrt{1+i_{f1}}+1\right)\right] \tag{2.17}$$

$$V_{PA} = \phi_t\left[2 \cdot \sqrt{1 + i_{f1}} + 5 + ln\left(\sqrt{1 + i_{f1}} + 1\right)\right] \tag{2.18}$$

Similarly, we can apply the UICM equation to the transistor M3 in (2.19).

$$V_{P3} = \phi_t\left[\sqrt{1 + i_{f3}} - 2 + ln\left(\sqrt{1 + i_{f3}} + 1\right)\right] \tag{2.19}$$

Lastly making $V_{P3} = V_{PA}$ one can solve for i_{f3} and with addiction of a planned I_{bias} calculate the appropriate aspect ratio for M3. The important part of these calculations is to pay attention to equations (2.18) and (2.19) to notice their equality is independent of the thermal voltage ϕ_t and, therefore, a temperature independent bias circuit.

2.1.2 Verifying the inversion level

Using the ACM model the inversion level of a transistor becomes one of the most important parameters to be designed, therefore most of the time it will be determined theoretically before the circuit implementation on a simulation-ready schematic. That makes its measurement important to determine if the parameters acquired are accurate and to make sure the transistors are operating in the correct inversion level.

One value that can hint towards the inversion level of a transistor is its GM/ID parameter. As we can see from equation 2.14 the GM/ID is inversely proportional to the inversion level that makes so the maximum possible value for it determined by $\frac{1}{n\phi_t}$ with the slope factor n being related to the technological node, something that makes a lot of sense. So by a rule of thumb, you can always correlate a higher GM/ID with a weaker inversion level and a lower GM/ID with a stronger inversion level. How high or how low is something that is going to change slightly between technologies so that's important for the designer to pick up.

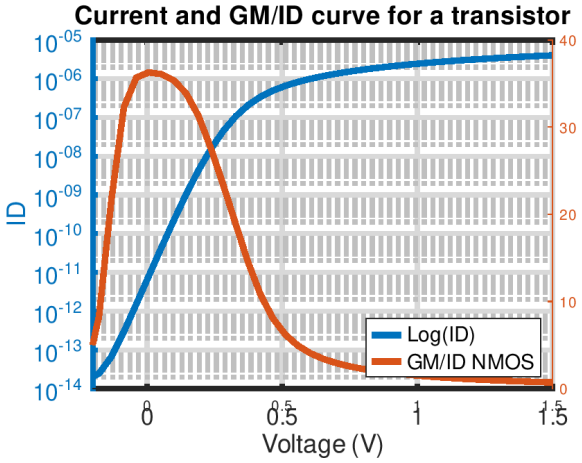

Figura 2 – Gm/Id curve and the drain current.

Source: Author

By making the gm/id simulation you can obtain the curves from figure 2 and interpret accordingly. Looking at the blue current curve we can spot the three operating regions of the saturated MOSFET the rightmost one being the strong inversion region, the leftmost being the weak inversion region and the transition region between them called the moderate inversion region. looking at those graphs one can deduct thresholds to differentiate the operating regions associating it with the matching gm/id value.

2.2 Basic building blocks

For this section, there will be a brief explanation of the operational principles of a few basic building blocks for power management units.

2.2.1 Rectifier

The process of converting an alternating current AC into a direct current DC is called rectification. The rectifier block is used to convert a bidirectional signal AC into a unidirectional DC supply, and this is done through the basic property of the diode that can only conduct when it is forward biased and blocks the current flow when it is reversed biased.

When the input signal that usually comes from an antenna is not a differential signal an extra block or external device is needed in order to convert the DC voltage into AC. The most common device that fullfills that need is called a balun. The balun isolates input signal into two output signal each with half amplitude and 180° phase shift. (WANG; LEE, 2018).

2.2.1.1 Dickson charge pump

One of the most common topologies for voltage multipliers or rectifiers is the Dickson charge pump for the reason that it presents a good trade-off between simplicity and efficiency. In figure 3 there is the description for an N-stage Dickson voltage rectifier.

Considering only the first stage of the rectifier represented by the source V_{in}, diodes D1 and D2 and capacitors C1 and C2, we can simplify the analysis of the circuit. When the input voltage V_{in} is negative the capacitor C2 is charged through the diode D1, when the input voltage becomes positive the capacitor C1 stores the resulting charges from the sum of the input voltage plus the voltage across C2 via the diode D2.

From (CARDOSO; SCHNEIDER; MONTORO, 2010) we have the following simplified design equations.

$$V_L = V_{PP} - n\phi_t ln\Big[\sqrt{\frac{2 \cdot \pi \cdot V_{PP}}{n \cdot \phi_t}}\Big(1 + \frac{I_L}{I_S}\Big)\Big] \tag{2.20}$$

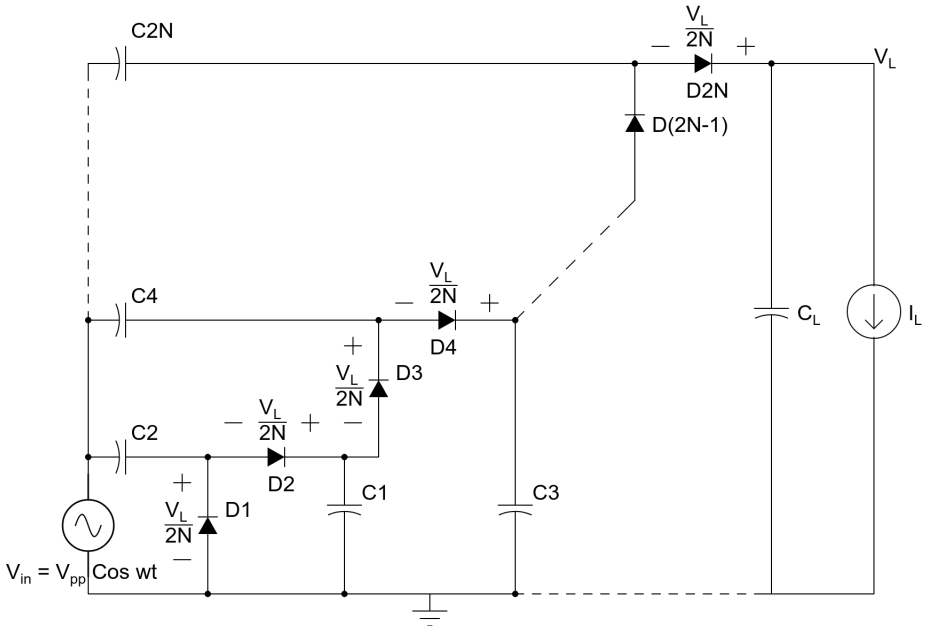

Figura 3 – N-stage voltage multiplier

Source: Author

$$I_o = \mu_0 n C'_{ox} \phi_t^2 e^1 \tag{2.21}$$

$$I_S = \frac{W}{L} I_o \cdot e^{\frac{-V_{T0}}{n \cdot \phi_t}} \tag{2.22}$$

Where V_L is the load or output voltage, V_{PP} is the peak value of the input voltage, n is the slope factor, ϕ_t is the thermal voltage, I_L is the load voltage and I_S, is the diode saturation current.

The equation (2.20) is used to determine the appropriate I_S given the circuit requirements and then (2.22) to find the transistor aspect ratio that satisfies the saturation current found.

2.2.1.2 Cross-coupled rectifier

The differential-drive cross coupled rectifier is a topology designed to reduce the turn-on threshold voltage and reverse leakage current from the diode connected MOSFETs.

The topology is described in Fig. 4 and is essentially made up of a pair of DC capacitors and cross-coupled transistors. With a fully differential sinusoidal input signal, the rectifier charges C_L through C_C in a start-up process. Eventually, V_O will settle to a level where the charge dissipated by the load resistor R_L and the charge delivered to CL in one cycle are equal. When the transistors are designed for the same conduction current, the common mode DC gate voltages of the transistors (V_X and V_Y) will settle to $\frac{V_0}{2}$ and can be seen in more detail in Fig. 5.

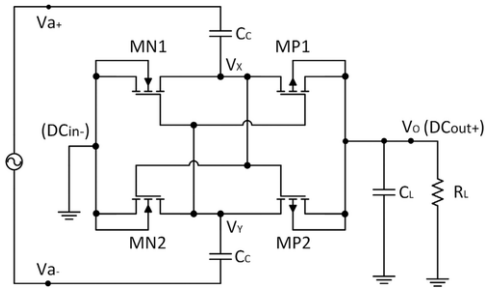

Figura 4 – Cross-coupled rectifier topology

Source: (LIANG; YUAN, 2019)

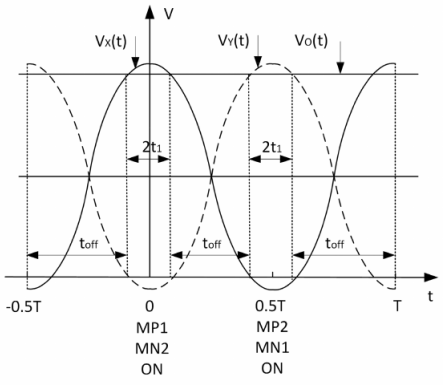

Figura 5 – Cross-coupled transistors activation over input voltage cycle.

Source: (LIANG; YUAN, 2019)

As seen in Fig. 5 the four transistors are controlled by the difference between the gate-source voltages as $V_{diff} = V_X - V_Y$ and operate in two separate groups. When the input voltage enters the positive cycle, the gate-source voltages of MP1 and MN2 increase with the differential signal. Once V_{diff} reaches V_{th}, MP1 and MN2 turn on. As V_{diff} stays over V_{th}, V_{a+} charges the load C_L and $Va-$ charges the bottom C_C. For V_{diff} between $-V_{th}$ and $+V_{th}$ all the transistors are kept off.

2.2.2 Folded Cascode amplifier

The basic idea behind a folded cascode topology is to, without adding a second amplifying stage, reach a high input and output impedance through cascode mirrors. The folding comes in handy as to fold the current nodes in a way so the output voltage swing isn't too affected by the current mirrors voltage drops as happens in the telescopic amplifier. There are several approaches to folded cascode amplifier topologies in Fig. 6 we can see one of the classical folded cascode topology that was used as an example in (ASSAAD; SILVA-MARTINEZ, 2009).

In this topology the same current I_b passes through all transistors apart from M0, M3 and M4 where the current is $2I_b$, and this makes calculations as the Slew Rate easier.

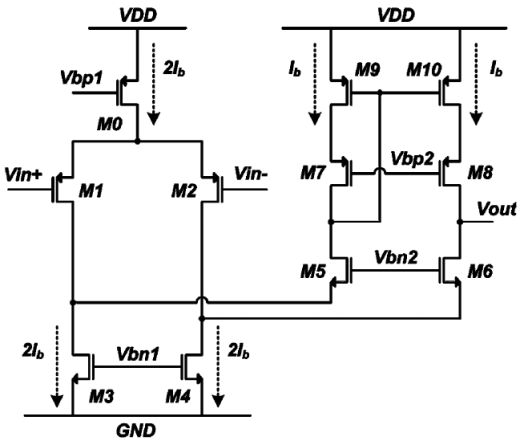

Figura 6 – Classical folded cascode amplifier

Source: (ASSAAD; SILVA-MARTINEZ, 2009)

2.2.3 Current reference

A current source is the electronic circuit element responsible for generating a constant current that keeps steady regardless of the load attached to it (LEE; SáNCHEZ-SINENCIO, 2021). In CMOS analog circuit design, current sources are essential for a variety of applications, such as biasing transistors, generating reference currents, and implementing active loads.

There are lots of different topologies that could be used to generate a current reference, and for this work, we are going to develop a self-biased current source (SBCS) shown in figure 7 as further described in (CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER, 2005).

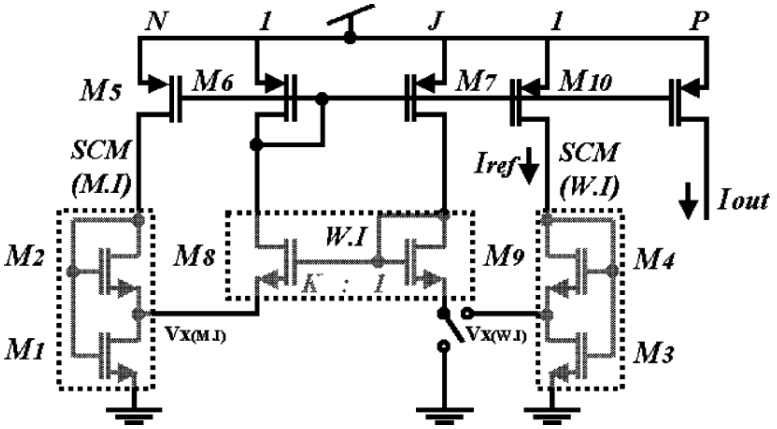

Figura 7 – Self Biased current source

Source: (CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER, 2005)

The way this topology works is based on two Self-Cascode Mosfet (SCM) that works on different inversion levels. on figure 7 we have the left SCM branch operating on moderate inversion while on the other side, the SCM works in weak inversion. The different

inversion levels on each SCM are designed in a way that their current versus voltage graphs cross each other on a point of interest where they both have the same output voltage. This point of equilibrium is what makes the SBCS viable and to properly design it one can apply the ACM formulas to the different SCM blocks making the operating voltage equal while setting the different inversion levels on the SCM transistors. An in-depth analysis of the equations used in the design is presented in both (CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER, 2005) and (STORCK, 2019).

3 Design and results

In this chapter the development of the circuits mentioned earlier is described and the graphical results properly explained.

3.1 Rectifier circuits design

The rectifier circuits designed in the following topics had a few specs that needed to be fulfilled as an output voltage of around 1.8 V, within a small area with a small ripple for an input signal being a 0.5 V 900 MHz differential signal.

3.1.1 Dickson Rectifier

The Dickson rectifier circuit was developed using the main idea from (CARDOSO; SCHNEIDER; MONTORO, 2010) using diode connected 0 VT transistors, where the bulk is connected to the drain in the "DTMOS"configuration. The transistors aspect ratio appeared to have an optimum size for maximum output voltage given the set input signal, allied with a load of a 1 pF capacitor in parallel with a 100 KΩ resistor. To reach the output voltage of 1.8 V 6 stages were necessary, and the topology can be seen in Fig. 8.

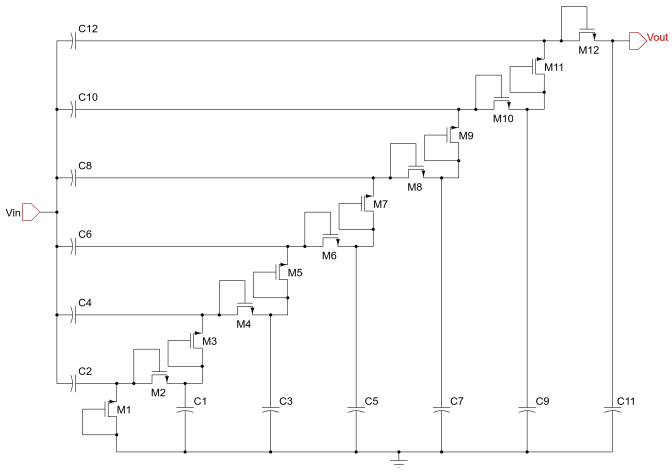

Figura 8 – Dickson rectifier circuit

Source: Author

3.1.1.1 Simulations and results

The main concerns about a rectifier circuit are the settling time, output voltage as well as the output voltage ripple. All those aspects can be inspected in Figures 9 and 10.

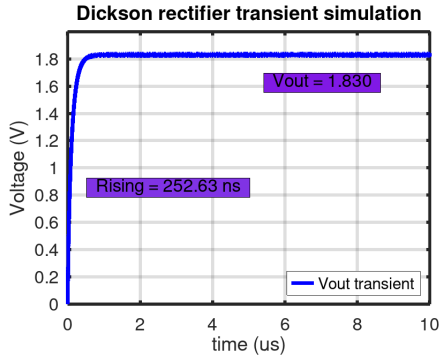

Figura 9 – Dickson rectifier start-up

Source: Author

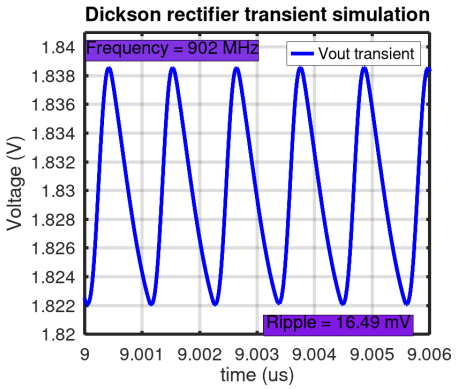

Figura 10 – Dickson rectifier frequency and ripple

Source: Author

The rise time archived with the circuit was 252.63 ns and the transient simulation was extended to 10 μs to guarantee a more stable output voltage result. The average voltage of 1.830 seems appropriate at typical conditions. Process-Voltage-Temperature (PVT) variations resulted in a minimum of 1.445 V at a SS corner and a maximum of 1.954 V for the FF corner. For the frequency, it is no surprise that the input frequency remained basically unchanged at the output, as it is not the circuit intent to change it. And lastly, the output voltage ripple of 16.49 mV means a $\pm$0.45% variation to the output voltage, so it might also be acceptable.

3.1.2 Cross-coupled Rectifier

To reach the aimed output voltage of 1.8 V 3 rectifying stages were necessary, and the topology is shown in Fig. 11.

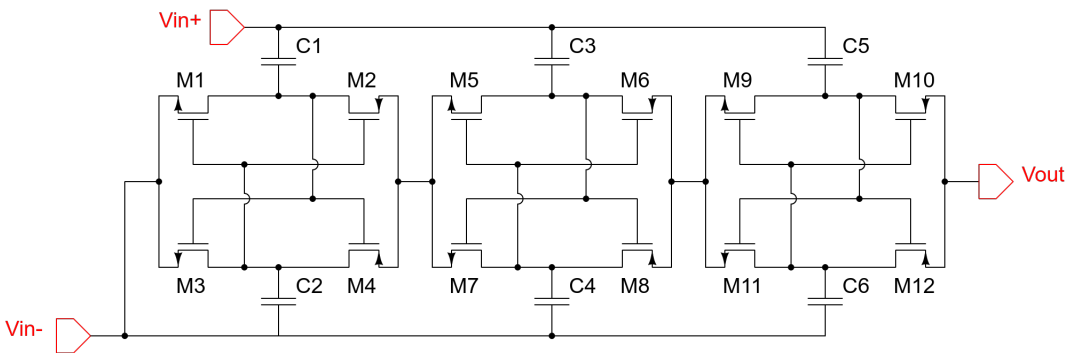

Figura 11 – 3 stage cross-coupled rectifier

Source: Author

Even though a theoretical analysis as made in (LIANG; YUAN, 2019) could provide a design methodology for the best efficiency for the transistors operating in weak and strong inversion levels, other studies as ((KOTANI; ITO, 2009))show that for ex-

perimental results there might be optimum transistor sizes related to output loads and technological parameters.

3.1.2.1 Simulations and results

The aspect ratios of the NMOS transistors (odd) and PMOS transistors (even) as well as the capacitors are described in table 1. As the transistor's size were chosen for the highest possible output voltage, the inversion level or saturation current weren't taken into account.

Device	Aspect Ratio	Parameter
Odd transistors (NMOS)	25	$\frac{0.5\mu}{0.18\mu} \times 9$
Even transistors (PMOS)	52.78	$\frac{1.9\mu}{0.18\mu} \times 5$
Capacitor 1 to 12	60 μ x 60 μ	412 fF

Tabela 1 – Cross-coupled device aspect ratios

Source: Author

This particular design was made with the intent to be used in an energy harvesting PMU block for an actual tape out. For that reason, there was the need to further investigate the behavior of the circuit in the Process-Voltage-Temperature corners. The output voltage and settling time can be seen in Tables 2 and 3.

PVT	Temperature			
Process	0º	27º	100º	Voltage
SS	1.236	1.365	1.584	450 mV
	1.687	1.765	1.899	500 mV
	2.063	2.100	2.168	550 mV
TT	1.499	1.567	1.702	450 mV
	1.876	1.903	1.965	500 mV
	2.163	2.171	2.199	550 mV
FF	1.697	1.716	1.754	450 mV
	1.978	1.975	1.982	500 mV
	2.213	2.202	2.191	550 mV

Tabela 2 – Output voltage corners simulated for the Cross-coupled rectifier

Source: Author

From the tables, we can spot the best and worse case scenarios for the output voltage and settling time. More specifically, we have the worst case for both the output voltage and settling time in the (SS, 0º, 450 mV) corner with respectively 1.24 V and 134 ns. As for the best case for the rising speed it is the (FF, 100º, 550 mV) corner sitting at 45.87 ns as expected from the FF (Fast Fast) corner. For the greatest output voltage it is the (TT, 100º, 550 mV) corner with an output of 2.2 volts.

As for the typical simulations on Fig. 12 the start-up waveform can be seen. In Fig. 13 the output voltage ripple is shown.

PVT	Temperature			
Process	0º	27º	100º	Voltage
SS	133.9 n	117.3 n	100.3 n	450 mV
	103.9 n	97.3 n	83.65 n	500 mV
	84.77 n	80.31 n	71.4 n	550 mV
TT	117.3 n	101.67 n	80.28 n	450 mV
	85.87 n	78.08 n	65.88 n	500 mV
	66.99 n	63.66 n	56.97 n	550 mV
FF	90.33 n	80.34 n	63.62 n	450 mV
	68.1 n	63.63 n	53.63 n	500 mV
	56.98 n	53.69 n	45.87 n	550 mV

Tabela 3 – Rising or start-up delay for the output to reach 90% of the steady state voltage

Source: Author

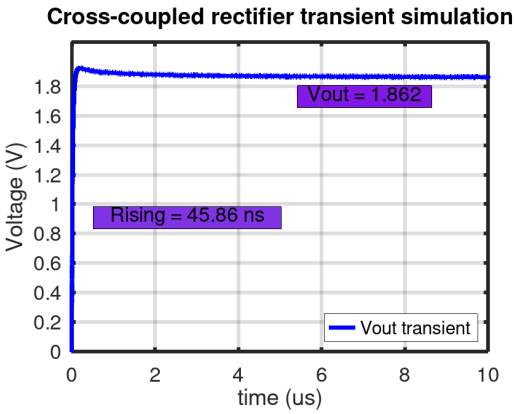

Figura 12 – Cross-coupled rectifier start-up

Source: Author

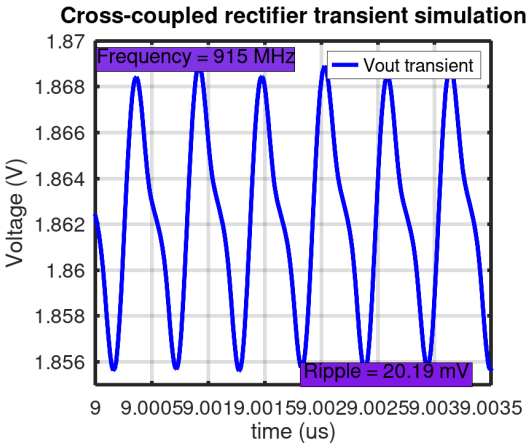

Figura 13 – Cross-coupled rectifier ripple

Source: Author

3.1.3 Comparison between the rectifier topologies

The decision to develop both topologies was specifically to measure and test which one could attend the given specifications better. With all the graphs generated we can have a fair comparison between the achieved results.

Comparing the 2 rectifier designs presented, it's clear to see that the rising time is way faster with the cross-coupled topology as well as a small advantage in the typical output voltage.

In favor of the Dickson topology we can see a more regular waveform, a slightly lower voltage ripple and a lower frequency distortion.

The decisive factor as to choose the cross-coupled rectifier on top of the Dickson charge pump is the circuit area. Analyzing one single stage from each topology their areas are closely matched but as seen earlier for the Dickson charge pump 6 stages were necessary to reach the desired 1.8 V as for the cross-coupled only 3 stages were enough.

This makes so the Dickson charge pump would have double the area of the cross-coupled rectifier.

3.1.4 Layout

The final step of the development of CMOS analog circuits is to design the block's layout. This is done by following several procedures as the DRC and LVS. The minor details involved in such processes won't be discussed further in this thesis but we can see in the next few paragraphs a brief explanation of what each of them is.

A DRC (Design Rule Check) is a process that ensures compliance between the generated layout and the specified design rules for the fabrication process being used. It involves checking the parameters as the minimum spacing between components, widths, and several other constraints for the different fabrication layers. This analysis is performed with the aid of specialized software tools that flag any violations, allowing the designer to adjust the layout accordingly.

A LVS (Layout vs Schematic) is a process that verifies if the designed layout matches the intended schematic design. This analysis is also performed with the aid of specialized software tools to check for discrepancies and identify errors.

The final result of the design can be seen in figure 14 highlighted in red. At the current moment when this thesis is being written the developed chip still hasn't been fully manufactured so it is uncertain if the physical IC met the desired specifications.

3.2 Folded cascode amplifier design

This section presents the design of a folded cascode amplifier as shown in Fig. 15. The topology shown in Fig. 15 is a classical folded cascode amplifier with PMOS differential input. The current mirror formed by transistors M3 & M4 was replaced with a 2 stage simple auto biased cascode current mirror (M3a & M4a, M3b & M4b) to improve the output resistance and therefore the gain. In usual strong inversion circuits this simple cascode could greatly reduce the output voltage swing because of the required $V_{DS,sat}$ but as this circuit is meant to work in weak inversion the $V_{DS,sat}$ from equation (2.10) results in a voltage drop below 200 mV for each stage. The current mirror formed by transistors M7 & M8 was also replaced but instead of a simple cascode it was for a low voltage cascode mirror (M7a & M8a, M7b & M8b) to again, improve the output resistance and therefore the gain.

The first step for the design was to find the appropriate transconductance to match the desired GBW from equation (3.1).

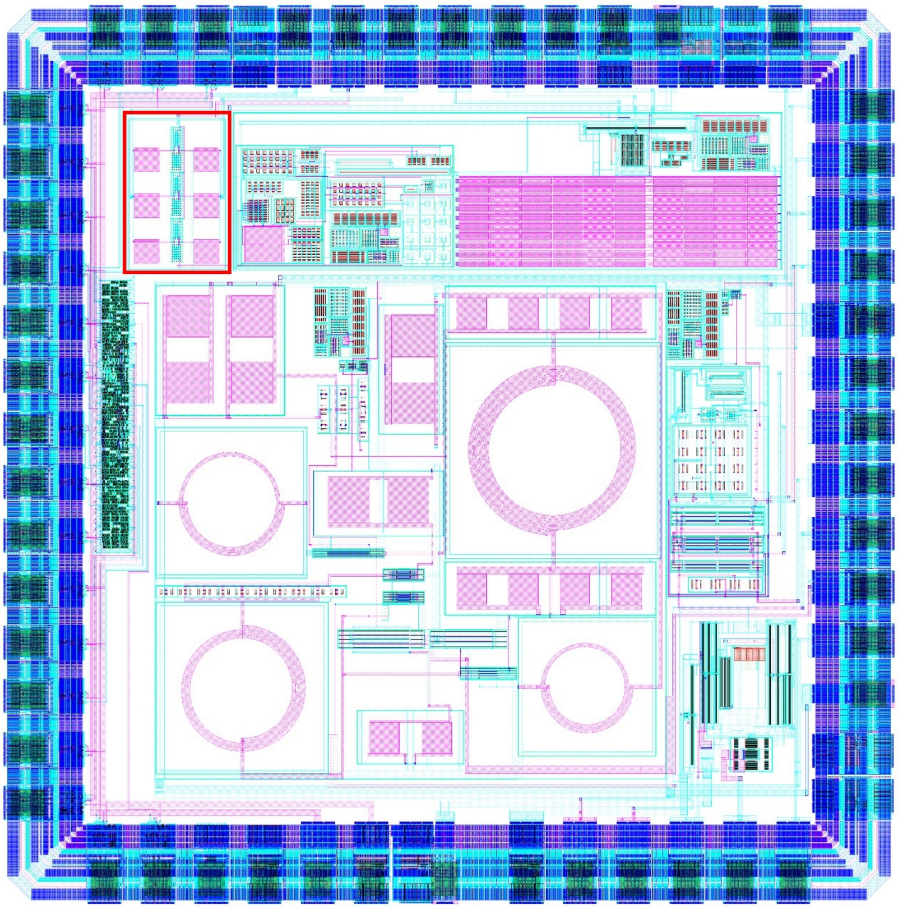

Figura 14 – Final design of the cross-coupled rectifier highlighted in red

Source: Author

$$g_{m1} = 2 \cdot \pi \cdot GBW \cdot C_L \tag{3.1}$$

For a GBW of 10 MHz and a $C_L = 407$ fF using equation (3.1) we approx the resulf of $g_{m1} \approx 25.57$ μA. Being g_{m1} the transconductance of the differential pair it is common to have it in the weak inversion region so using equation (2.13) and choosing an apropriate iversion level $i_f \approx 0.25$ we have the following (3.2) using $n = 1.207$ and $\phi_t = 25.86$ mV.

$$\frac{g_{m1}}{I_{D,M1}} = \frac{1}{n \cdot \phi_t} \frac{2}{\sqrt{1 + 0.25} + 1} \tag{3.2}$$

For the transconductance criteria the minimun current flowing through M1 sits arround 900n.

To simplify the slewrate calculation in this design lets assume the common folded cascode configuration with the currents $I_{D,M9} = I_{D,M7} = I_{D,M8}$ so the resulting Slew rate is described in equation (3.3). As for the Slew rate value lets try to make it over 5 V/μs so the minimun current for M9 would be 2.035 μA. To give it a bigger margin we choose

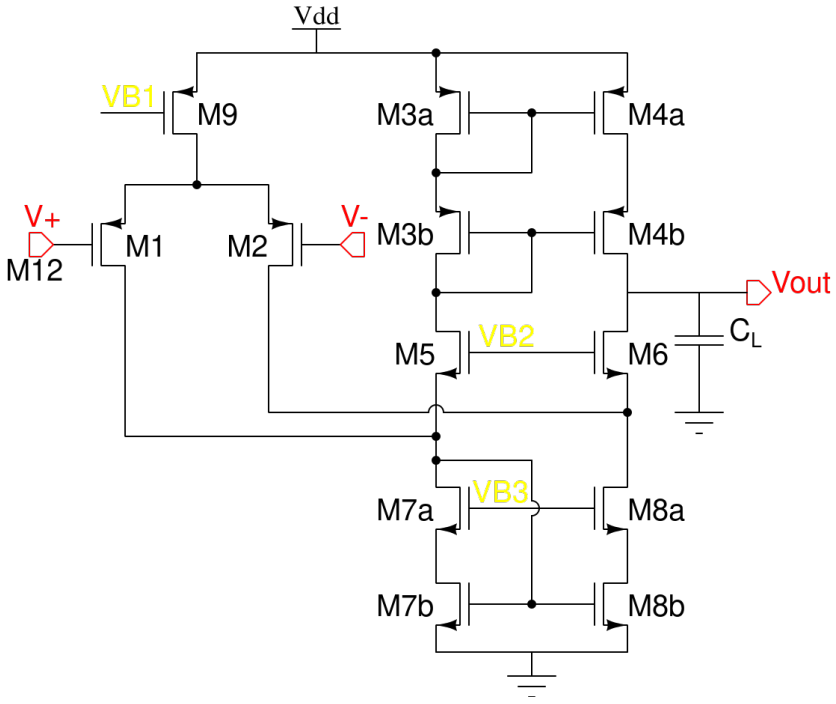

Figura 15 – Folded cascode amplifier topology.

Source: Author

$I_{D,M9} = 5\ \mu$A and also set the inversion levels of all other transistors (apart from the bias circuit) to work on weak inversion with $i_f \approx 1$.

$$S_L = \frac{I_{D,M10}}{C_L} \tag{3.3}$$

With all the transistor inversion levels and respective currents set their aspect ratios are calculated as in (2.7) with the saturation condition($i_r \to 0$) and are described in table 4.

Transistor	I_D	Inversion Level	Aspect Ratio	$\frac{W}{L}$
M1 & M2	2.5 μA	0.25	100	$\frac{100\mu}{2\mu} \times 2$
M3* & M4*	2.5 μA	1	60	$\frac{24\mu}{2\mu} \times 5$
M5 & M6	2.5 μA	2	11	$\frac{4.4\mu}{2\mu} \times 5$
M7* & M8*	5 μA	2	22	$\frac{8.8\mu}{2\mu} \times 5$
M9	5 μA	1	120	$\frac{48\mu}{2\mu} \times 5$

Tabela 4 – Folded cascode transistor aspect ratio

Source: Author

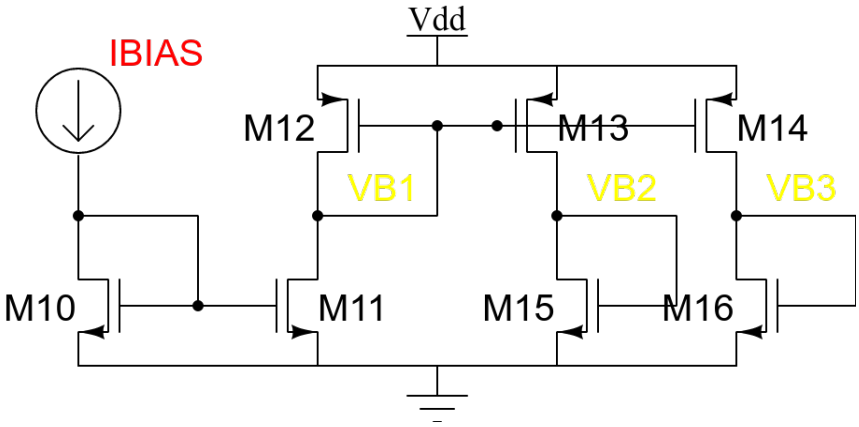

Figura 16 – Bias network circuit to generate VB1, VB2 and VB3.

Source: Author

To generate the appropriate bias voltages, we have the bias network shown in Fig. 16. The first step was to choose the bias current that passes to the mirror M12, M13 and M14. Setting this bias current as a fraction of the current on the rest of the circuit made sense power wise, so it was set as 1 μA. Assuming a bias current of 100 nA M10 and M11 have a 1:10 ratio. For the size of M12 & M13 & M14 the aspect ratio should be 5 times smaller to adjust the current in M9. For the bias voltages generated by M15 and M16 the inversion levels and aspect ratios were calculated based on the UICM equations as previously done in the current mirror subsection for the values of $i_{f15} \approx 77$ and $i_{f16} \approx 144$ their full specs are presented in Table 5.

Transistor	I_D	Inversion Level	Aspect Ratio	$\frac{W}{L}$
M10	100 nA	5	0.345	$\frac{0.69\mu}{4\mu} \times 2$
M11	1 μA	2.78	3.105	$\frac{0.69\mu}{4\mu} \times 18$
M12 & M13 & M14	1 μA	0.36	24	$\frac{48\mu}{2\mu}$
M15	1 μA	143.49	0.06	$\frac{0.48\mu}{8\mu}$
M16	1 μA	77.32	0.1125	$\frac{0.45\mu}{4\mu}$

Tabela 5 – Bias network transistor aspect ratios

Source: Author

3.2.1 Simulations and results

The gain and phase of the output signal was obtained through an AC simulation and the results can be seen in Fig. 17 and Fig. 18.

Considering the parameters aimed as 10 MHz GBW and arroud 60º of phase margin the circuit does behave about right. For the DC gain the higher the better so 95 Db is a pretty acceptable result.

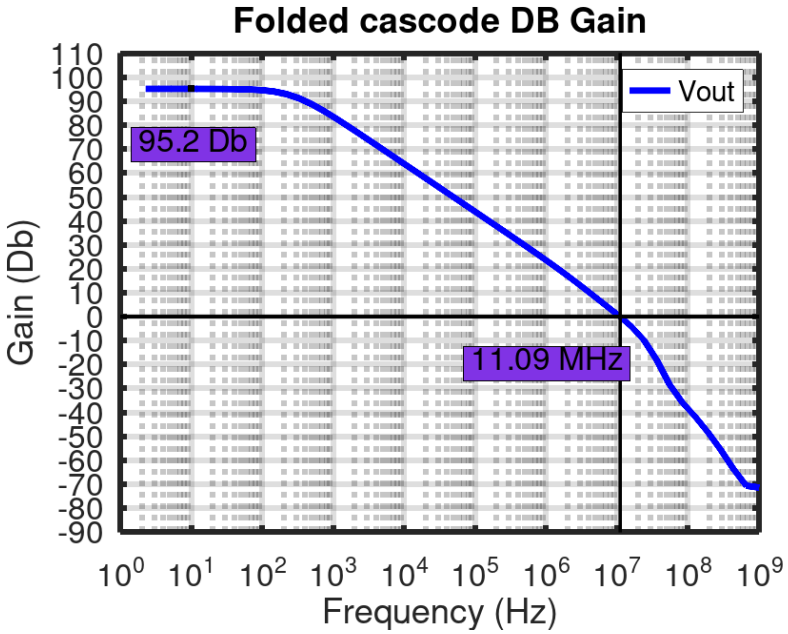

Figura 17 – Folded cascode DC Gain and UGBW

Source: Author

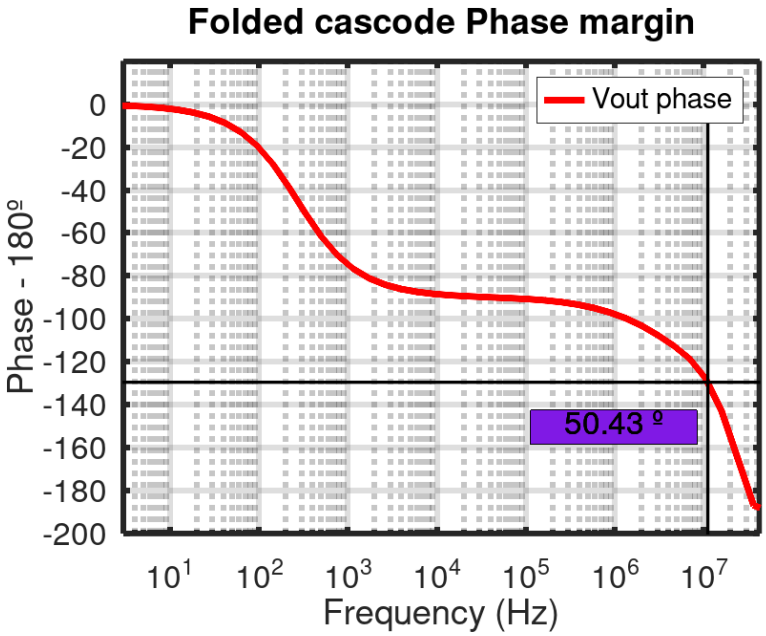

Figura 18 – Folded cascode phase margin

Source: Author

Another few important parameters for an operational amplifier is the Power Source Rejection Rate and Slew Rate that can be seen in Fig. 19 and 20.

For those parameters the PSRR at DC level of about -95 Db is a decent result as for the Slew rate we can't really say the same as the desired value was at least over 5 v/ μs. It's estimated that the slight variations in the tail current might have impacted the slew rate result as the rising and falling rates are supposed to be equal but as we can see

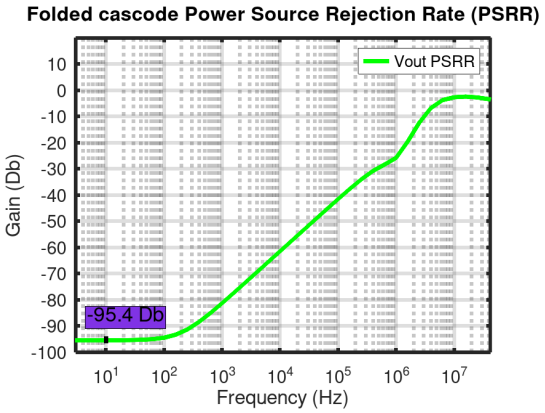

Figura 19 – PSRR in Db

Source: Author

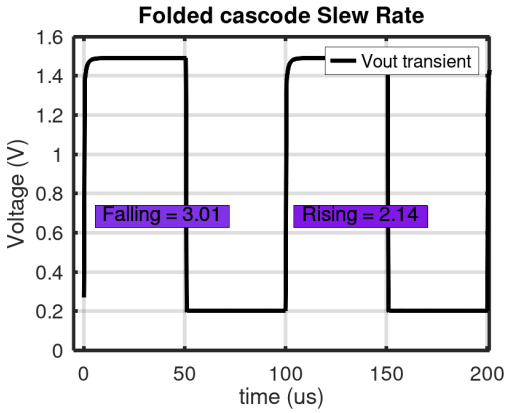

Figura 20 – Slew rate given in V/μs

Source: Author

from Fig. 20 they aren't really the same.

3.3 SBCS

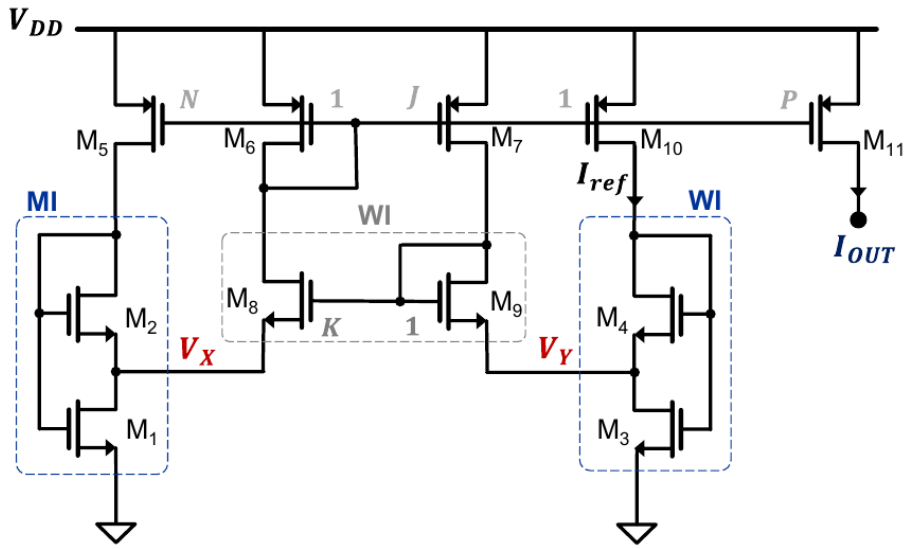

Figura 21 – SBCS designed

Source: (ADORNES et al., 2022)

This section presents the design of an SBCS(Self-biased current source). The first step in the design was to select an output current as it is the current source's most important parameter. The parameter decided was an output current of 1 uA. With that out of the way, a few assumptions were made to start the design process. First, the aspect ratios of both transistors on the MI(Moderate inversion) SCM were equal. second, the inversion level for the MI SCM was going to be around 10 and the inversion lever for the WI SCM is going to be around 0.1.

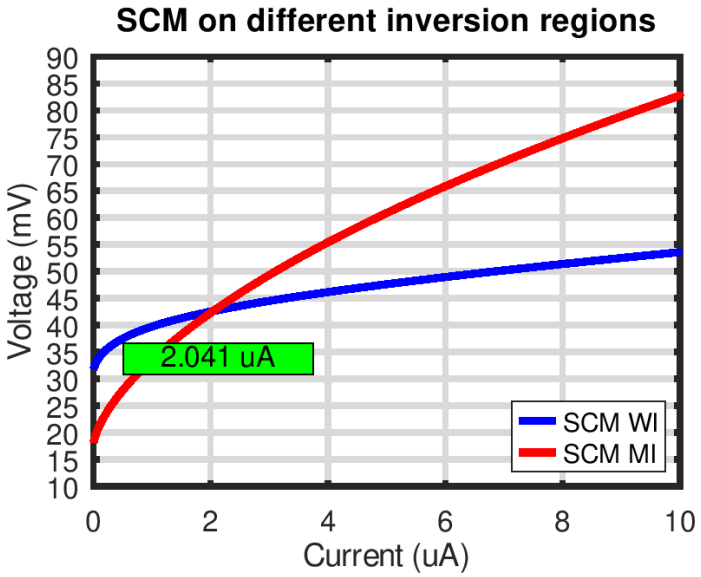

Figura 22 – Voltage vs current graphs for the SCM blocks

Source: Author

We can clearly see on figure 22 what the voltage vs current graphs of the SCM blocks looks like, and we can also see that they cross at the point of interest of $\approx 2\mu A$ in about 43 mV. The point of interest diverges from the desired output current as that was the number found after applying the theoretical aspect ratios found to the transistors. Even through not ideal this result is still valid as it was in a close range for correction with the output current mirror ratios.

On figure 21 we can see the topology where the mirror multipliers are mostly equal one (N, J, K) except for the output mirror (P) that has half the size of the others as the circuit is designed to reach the equilibrium with $2\mu A$ where the output current is supposed to be $1\mu A$. Using this strategy we can make the output mirrors smaller for circuits that could need several of them.

3.3.1 Simulations and results

In table 6 we can see all the transistor's aspect ratios and their appropriate inversion levels of the final schematic.

With the circuit we then could simulate it to its limits varying the operating temperature and as a result, we got the curves from figure 23 where the temperature varies between -40ºC and 100ºC with a DC sweep of the VDD voltage from 0 to 1.8 Volts.

From figure 23 we can observe how much the output current varies regarding different operating temperatures and for the look of it it seems like the results are appropriate. Even though the established output current requirement was 1 μA the result of 1.101 μA seems about right for room temperature operation.

Transistor	I_D	Inversion Level(if)	Aspect Ratio	$\frac{W}{L}$
M1	2.2 μA	10.14	1.667	$\frac{5\mu}{3\mu}$
M2	4.4 μA	20.28	1.667	$\frac{5\mu}{3\mu}$
M3	4.4 μA	1.8	19.4	$\frac{19.4\mu}{1\mu}$
M4	2.2 μA	0.227	77.6	$\frac{19.4\mu}{1\mu} \times 4$
M5 & M6 & M7 & M10	2.2 μA	150.5	0.32	$\frac{0.4\mu}{10\mu} \times 8$
M8 & M9	2.2 μA	1.923	9	$\frac{5\mu}{10\mu} \times 18$
M11(output)	1.1 μA	305.7	0.16	$\frac{0.4\mu}{10\mu} \times 4$

Tabela 6 – SBCS transistor aspect ratios and inversion levels

Source: Author

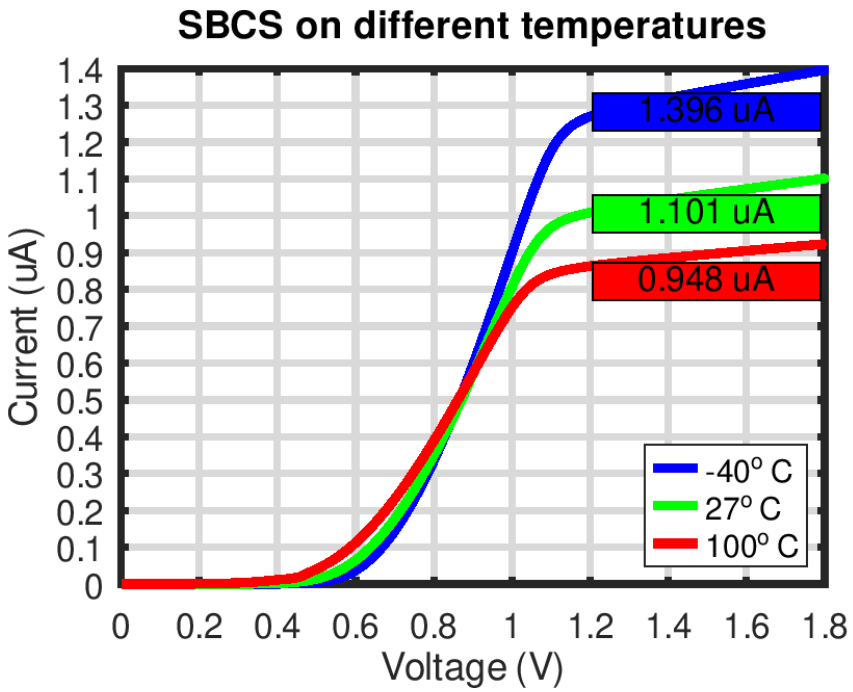

Figura 23 – Temperature curves for the output current

Source: Author

4 Conclusion

The proposed circuits were designed, simulated and validated in comparison with the established requirements, reaching most of the desired values and therefore completing the proposed objectives.

This thesis completed its goals by detailing the design process involved in the development of the presented blocks and providing a better viewpoint regarding the design steps involved in the development of analog circuits included in integrated chip fabrication processes.

For future work based on this thesis it is possible to speculate the possibility of the construction of a more complex integrated circuit made by a combination of the ones shown here along with other blocks, an example of such an application could be a DC-DC Buck converter powered by energy harvesting.

Referências

ADORNES, C. M. et al. Bridging the gap between design and simulation of low-voltage cmos circuits. *Journal of Low Power Electronics and Applications*, v. 12, n. 2, 2022. ISSN 2079-9268. Disponível em: <https://www.mdpi.com/2079-9268/12/2/34>. Citado 3 vezes nas páginas 25, 27 e 44.

ASSAAD, R. S.; SILVA-MARTINEZ, J. The recycling folded cascode: A general enhancement of the folded cascode amplifier. *IEEE Journal of Solid-State Circuits*, v. 44, n. 9, p. 2535–2542, 2009. Citado 2 vezes nas páginas 31 e 32.

CAMACHO-GALEANO, E.; GALUP-MONTORO, C.; SCHNEIDER, M. A 2-nw 1.1-v self-biased current reference in cmos technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, v. 52, n. 2, p. 61–65, 2005. Citado 2 vezes nas páginas 32 e 33.

CARDOSO, A. J.; SCHNEIDER, M. C.; MONTORO, C. G. Design of very low voltage cmos rectifier circuits. In: *2010 2nd Circuits and Systems for Medical and Environmental Applications Workshop (CASME)*. [S.l.: s.n.], 2010. p. 1–4. Citado 2 vezes nas páginas 29 e 35.

CUNHA, A.; SCHNEIDER, M.; GALUP-MONTORO, C. An mos transistor model for analog circuit design. *IEEE Journal of Solid-State Circuits*, v. 33, n. 10, p. 1510–1519, 1998. Citado na página 25.

DANCY, A.; AMIRTHARAJAH, R.; CHANDRAKASAN, A. High-efficiency multiple-output dc-dc conversion for low-voltage systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, v. 8, n. 3, p. 252–263, 2000. Citado na página 19.

DAS, S. K. Battery and power management unit design. In: _____. *Mobile Terminal Receiver Design: LTE and LTE-Advanced*. [S.l.: s.n.], 2017. p. 317–336. Citado na página 19.

GALUP-MONTORO, C. et al. The advanced compact mosfet (acm) model for circuit analysis and design. In: *2007 IEEE Custom Integrated Circuits Conference*. [S.l.: s.n.], 2007. p. 519–526. Citado na página 25.

HELLA, M. M.; MERCIER, P. (Ed.). *Power Management Integrated Circuits (Devices, Circuits, and Systems)*. Kindle edition. [S.l.]: CRC Press, 2016. 347 p. Citado na página 19.

KOTANI, K.; ITO, T. High efficiency cmos rectifier circuits for uhf rfids using vth cancellation techniques. In: *2009 IEEE 8th International Conference on ASIC*. [S.l.: s.n.], 2009. p. 549–552. Citado na página 36.

KRUISKAMP, W.; BEUMER, R. Low drop-out voltage regulator with full on-chip capacitance for slot-based operation. In: *ESSCIRC 2008 - 34th European Solid-State Circuits Conference*. [S.l.: s.n.], 2008. p. 346–349. Citado na página 19.

LEE, S.; SáNCHEZ-SINENCIO, E. Current reference circuits: A tutorial. *IEEE Transactions on Circuits and Systems II: Express Briefs*, v. 68, n. 3, p. 830–836, 2021. Citado na página 32.

LIANG, Z.; YUAN, J. Modelling and optimisation of high-efficiency differential-drive complementary metal–oxide–semiconductor rectifier for ultra-high-frequency radio-frequency energy harvesters. *IET Power Electronics*, v. 12, n. 3, p. 588–597, 2019. Disponível em: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-pel.2018.5773>. Citado 2 vezes nas páginas 31 e 36.

SAFARI, N. *Design of a DC/DC buck converter for ultra-low power applications in 65nm CMOS Process*. Tese (Doutorado) — Linköping Institute of Technology, 2012. Disponível em: <http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-80395>. Citado na página 19.

STORCK, E. Tese (Graduação em Engenharia Elétrica), *Design de fonte de corrente auto polarizada*. 2019. Disponível em: <https://repositorio.ufsc.br/handle/123456789/200949>. Citado na página 33.

WANG, Y.; LEE, J.-C. A miniaturized marchand balun model with short-end and capacitive feeding. *IEEE Access*, v. 6, p. 26653–26659, 2018. Citado na página 29.

YASUDA, T.; YAMAMOTO, M.; NISHI, T. A power-on reset pulse generator for low voltage applications. In: *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*. [S.l.: s.n.], 2001. v. 4, p. 599–601 vol. 4. Citado na página 19.